Digital Systems: Problem sheet 5

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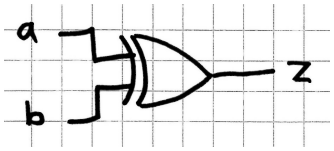
1 An XOR gate $z = a \oplus b$ has the following truth table:

a	b	z
0	0	0
0	1	1
1	0	1
1	1	0

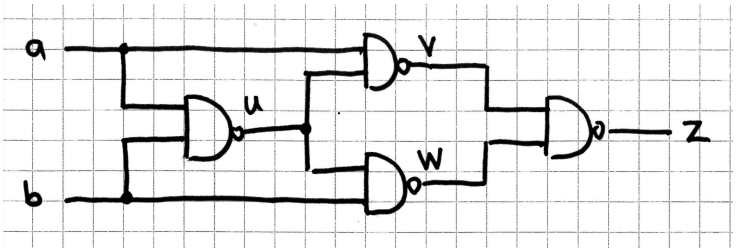


(a) Show that $\oplus$ is associative and commutative. Does it have an identity element?

(b) Show how to build an XOR gate from a 2-input OR gate, two 2-input AND gates and two inverters.

(c) Can you still build an XOR gate if one of the two AND gates is replaced by an OR gate?

(d) Show that the following circuit of four NAND gates also computes $z = a \oplus b$.



2 (a) Design a CMOS implementation of a NOR gate, with the following truth table.

a	b	z
0	0	1
0	1	0
1	0	0
1	1	0

(b) In the lecture, we designed a CMOS gate that computed the function

$$z = \neg((a \wedge b) \vee c).$$

Design a gate that computes

$$w = \neg((a \vee b) \wedge c)$$

instead.

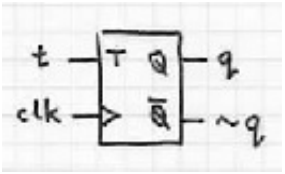
(c) What general principle relates part (a) with the CMOS NAND gate designed in lectures, and part (b) with the AND–OR–NOT gate designed there?

3 (a) Design a *clocked set/reset latch* with the following behaviour. There are two inputs a and b; if $a = 1$ at a clock edge, then the output z goes from 0 to 1. The output then remains at 1 until $b = 1$ at a clock edge, and then returns to 0. The behaviour if $a = b = 1$ at any clock edge can be whatever is easiest to implement.

(b) Enhance your design to produce an additional output w that receives a pulse for exactly one clock cycle whenever the circuit is triggered by an event with $a = 1$, but does not receive another pulse until the circuit has been reset by setting $b = 1$ at a clock edge.

4 A T-type flip-flop has a control input t, in addition to an edge-triggered clock input. If $t = 1$ at a clock edge, then the flip-flop changes state; otherwise it remains in the same state.

q_t	t	q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0



(a) Show how to construct a T-type flip-flop from a D-type flip-flop and an XOR gate.

(b) Show how to construct a synchronous binary counter from a row of T-type flip-flops and a row of AND gates. The counter should satisfy the specification $bin(a_{t+1}) \equiv bin(a_t) + 1 \pmod{2^n}$.

(c) Show how to construct a synchronous binary counter from a row of D-type flip-flops and a row of half-adders.

(d) Use your answer to part (a) to explain the connection between the circuit in parts (b) and (c).

5 Tests with an actual pull-cord light switch installed at the lecturer's home reveal that the light does not go on until the cord is released, but goes off as soon as it is pulled a second time. Modify the bathroom light-switch circuit to reproduce this behaviour.

6 In the lecture, it was shown that the set of connectives $\{\wedge, \vee, \neg\}$ is adequate to express any Boolean function, as is the singleton set {NAND}.

(a) Show that the singleton {NOR} is also adequate.

(b) Show that the set {XOR, ¬} is *not* adequate. *Hint: find a proper subset of the set of all Boolean functions of two variables x and y that contains x, y and the two Boolean constants and is closed under* XOR *and* ¬.

7 A *popcount circuit* has n Boolean inputs, and computes a binary number (with $\lfloor \log n \rfloor + 1$ bits) that counts the number of 1 bits among the inputs.

(a) Show how to construct a popcount circuit from a balanced tree of adders so that the combinational path from each input bit passes through $O(\log n)$ adders before reaching the output.

(b) If we use ripple-carry adders to implement the circuit, a k-bit adder has both size and worst-case delay that are linear in k. Use these facts to estimate the size and propagation delay of the popcount circuit.

(c) In fact, some of the delays in ripple-carry adders are smaller than the estimate $O(k)$, because for $i \le j$, the combinational path from the i'th pair of inputs to the j'th output has length proportional to $j - i + 1$. Use this fact to refine your estimate of the delay of the popcount circuit.

8 A bit-serial comparator has two inputs a and b. Successive binary digits of two numbers are presented at the two inputs on successive clock cycles, least significant bit first, and the circuit has two outputs L and G that indicate whether the number presented so far at a is less than or greater than the number presented at b (up to the preceding clock cycle); both outputs are zero if the numbers are equal so far. Thus, if the inputs at a and 0, 1, 1, 0 and those at b are 1, 0, 1, 1, then after 4 clock pulses the outputs are $L = 1$ and $G = 0$ because $6 = 0110_2$ is less than $13 = 1101_2$.

(a) If the current outputs are L_i and G_i and the current input bits are a_i and b_i, show how to compute the next outputs L_{i+1} and G_{i+1}.

(b) Use the previous part to give the design for a sequential circuit that inputs the numbers a and b and outputs L and G as described.

(c) What would change if the numbers a and b were presented with their most significant bit first?