[A]

Bits [11:8] × Bits [15:12]

	0,1	2,3	4,5	6,7	8,9	A,B	C,D	E,F	
0	LSLS i5				LSRS i5				LSLS/LSRS/ASRS r1, r2, #imm5
1	ASRS i5				ADDS r	SUBS r	ADDS i3	SUBS i3	ADDS/SUBS r1, r2, r3
2	MOVS i8				CMP i8				ADDS/SUBS r1, r2, #imm3
3	ADDS i8				SUBS i8				MOVS/CMP/ADDS/SUBS r1, #imm8
4	[B]				LDR pc				LDR r1, [pc, #4*imm8] (*aka* LDR r1, =const)
5	STR r	STRH r	STRB r	LDRSB r	LDR r	LDRH r	LDRB r	LDRSH r	STRx/LDRx r1, [r2, r3]
6	STR i5				LDR i5				STRx/LDRx r1, [r2, #s*imm5]
7	STRB i5				LDRB i5				
8	STRH i5				LDRH i5				
9	STR sp				LDR sp				STR/LDR r1, [sp, #4*imm8]
A	ADD pc				ADD sp				ADD r1, pc, #4*imm8 (*aka* ADR r1, label)
B	[C]								ADD r1, sp, #4*imm8
C	STM				LDM				STM/LDM r1!, {regs}
D	[D]								
E	B								B 2*disp11
F	[E]								

[B]

Bits [7:4] × Bits [15:8]

	0,1,2,3	4,5,6,7	8,9,A,B	C,D,E,F	
40	ANDS	EORS	LSLS	LSRS	op r1, r2
41	ASRS	ADCS	SBCS	RORS	
42	TST	NEGS	CMP	CMN	
43	ORRS	MULS	BICS	MVNS	
44	ADD				ADD/CMP/MOV r/h1, r/h2
45	CMP				
46	MOV				
47	BX		BLX		BX/BLX r/h1

[C]

Bits [7:4] × Bits [15:8]

	0,1,2,3	4,5,6,7	8,9,A,B	C,D,E,F	
B0	ADD sp		SUB sp		ADD/SUB sp, sp, #4*imm7
B1					
B2	SXTH	SXTB	UXTH	UXTB	SXTH/SXTB/UXTH/UXTB r1, r2
B3					
B4	PUSH				PUSH/POP {regs}
B5					
B6		CPS			CPSIE/CPSID i
B7					
B8					
B9					
BA	REV	REV16	REVSH		REV/REV16/REVSH r1, r2
BB					
BC	POP				
BD					
BE	BKPT				BKPT #imm8
BF	[F]				

[D]

Bits [15:8]

D0	BEQ	D8	BHI	Bcc 2*disp8
D1	BNE	D9	BLS	
D2	BCS, BHS	DA	BGE	
D3	BCC, BLO	DB	BLT	
D4	BMI	DC	BGT	
D5	BPL	DD	BLE	
D6	BVS	DE		
D7	BVC	DF	SVC	SVC #imm8

[E] 32-bit instructions:

F38? 88??	MSR special, r1
F3EF 8???	MRS r1, special
F3BF 8F4?	DSB
F3BF 8F5?	DMB
F3BF 8F6?	ISB
F000-F7FF B???/F???	BL 2*disp24

[F] Special instructions:

BF80	NOP
BF90	YIELD
BFA0	WFE
BFB0	WFI
BFC0	SEV