Digital Hardware
Problems 2

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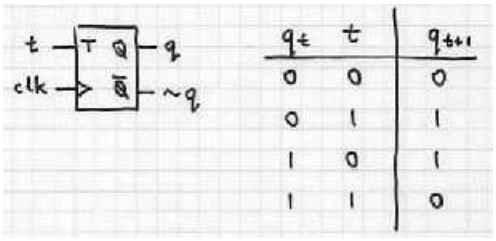
1 Draw the circuit diagram for a 4-bit carry-lookahead adder, leaving the carry status signals as single values drawn from the set $\{K, P, G\}$. Annotate each wire with the value it carries when the adder is performing the addition $3 + 9 = 12$.

2 Design a synchronous sequential circuit with two inputs a and b and a single output z. If $a = 1$ at a rising clock edge, the circuit produces an output pulse that lasts for one clock cycle. The circuit does not produce any more ouput pulses until it has been reset by setting $b = 1$ at a rising clock edge. The behaviour if both inputs are 1 simultaneously is not defined, but it must be possible to obtain an output pulse in every other clock cylce by setting $a = 1$ and $b = 1$ at alternate clock edges. Use positive edge-triggered D-type flip-flops in your design.



3 A T-type flip-flop has a control input t, in addition to an edge-triggered clock input. If $t = 1$ at a clock edge, then the flip-flop changes state; otherwise it remains in the same state.

(i) Show how to construct a T-type flip-flop from a D-type flip-flop and an XOR gate.

(ii) Show how to construct a synchronous binary counter from a row of T-type flip-flops and a row of AND gates.

(iii) Show how to construct a synchronous binary counter from a row of D-type flip-flops and a row of half-adders.

(iv) Use your answer to part (i) to explain the connection between the circuit in parts (ii) and (iii).

4 A bit-serial comparator has two inputs a and b. Successive binary digits of two numbers are presented at the two inputs on successive clock cycles, least significant bit first, and the circuit has three output x, y and z that indicate whether the number presented so far at a is less than, equal to, or greater than the number presented at b (up to the preceding clock cycle). Thus, if the inputs at a and 0, 1, 1, 0 and those at b are 1, 0, 1, 1, then after 4 clock pulses the outputs are $x = 1$, $y = 0$ and $z = 0$, because $6 = 0110_2$ is less than $13 = 1101_2$.

(i) Using the type

data *LEG* = *Lt* | *Eq* | *Gt*

define, in terms of *foldl*, a function

compare :: [*Bit*] → [*Bit*] → *LEG*

that compares two binary numbers presented LSB-first as lists of bits. [Hint: the answer is in a lecture handout.]

(ii) Devise a (symmetrical) representation of the three states *Lt*, *Eq*, *Gt* in two bits, and design output circuits that produce the three signals x, y and z.

(iii) Draw a state transition diagram that shows how the comparator moves between the three states *Lt*, *Eq* and *Gt* depending on the input bits a and b.

(iv) Using the state encoding from part (ii), derive a truth table for the next-state logic.

(v) Use Karnaugh maps to design the next-state logic for the comparator.